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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,796	04/09/2004	Christopher Boguslaw Kocon	018865-011710US	9334

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EXAMINER

WOJCIECHOWICZ, EDWARD JOSEPH

ART UNIT PAPER NUMBER

2815

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/821,796

Applicant(s)

KOCON, CHRISTOPHER  
BOGUSLAW

Examiner

Edward Wojciechowicz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-52 is/are pending in the application.
- 4a) Of the above claim(s) 11-17 and 38-52 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 18-37 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 08/04
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-10 and 18-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh et al (2003/0207538) in view of Minato (2005/0048701). Hshieh teaches the basic structure of the claimed invention with a Schottky diode integrated with a MOS device with charge control electrodes formed in trenches which are insulated from one another. See, for example, the configuration in Fig. 4 where polysilicon gates (210) are formed in an epitaxial semiconductor layer formed over a substrate, and insulated from the region by dielectric (206). Metal layer (216) forms a Schottky barrier with the semiconductor region. In addition, the metal layer (216) constitutes part of the anode of the device, while the lower electrode (218) forms the cathode electrode of the device. As discussed in [0050], the gates may be independently biased and their function would inherently be to form a uniform electric field in the device.

Since the gates may be formed in a stripe configuration [0002], the spaces between the gates can be considered to constitute a trench region with insulation (206) formed along the sides of the trench, but not along the bottom of the trench. As is known in the prior art (FIG. 3A), these trenches may typically terminate at an interface

between a semiconductor region and an epitaxial layer, and the Schottky diodes formed in the trenches can be reversed biased as discussed in [0002]. It is seen that Hshieh also forms diodes in these trench regions, as evidenced by the P-N junctions formed between regions (212), (204) and (202) in Fig. 4, and regions (212) can be considered to form shallow regions on each side of the trench in a top surface region of the semiconductor region, in contact with the metal layer.

Minato is cited to show alternate configurations for forming multiple diodes in trenches which are isolated by dielectric layers, as shown in FIG. 13, and taken together, these references teach all of the features of the invention. One would be motivated to combine these references to provide a more efficient integration of the multiple diodes in the device of Hshieh.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Wojciechowicz whose telephone number is (571) 272-1739. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Edward Wojciechowicz  
Primary Examiner  
Art Unit 2815

EW: ew